

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER OF PATENTS AND TRADEMARKS P.O. Box 1450 Alexandria, Viginia 22313-1450 www.uspto.gov

PAPER NUMBER

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/429,283	10/28/1999	SHUICHI UENO	0057-2534-2Y	5740
22850	7590 05/30/2003			
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			EXAMINER	
1940 DUKE STREET ALEXANDRIA, VA 22314		FOURSON III, GEORGE R		

ART UNIT

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PARTMENT OF COMMERC U.S. Patent and T. demark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

gr

APPLICATION NO./
CONTROL NO.

FILING DATE

FIRST NAMED INVENTOR /
PATENT IN REEXAMINATION

ATTORNEY DOCKET NO.

EXAMINER	

ART UNIT PAPER .

26

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The appendix to the Appeal Brief filed 5/20/02 contains the following errors in the listing of the claims on appeal. In claim 14, lines 12, 13 and 15, --active-- should appear before "region".

Please see attached copy of the translation of Japan '766.

The correct listing of the Prior Art of Record in the Examiner's Answer mailed 10/02/02 is as follows:

Kuroi, T., et al., "The Impact of Nitrogen Implantation into Highly Doped Polysilicon Gates for Highly Reliable and High-Performance Sub-Quarter-Micron Dual Gate Complementary Metal Oxide Semiconductor", Japanese Journal of Appl. Phys., Vol.34 (February 1995), pp.771-775

Sze, S.M., "VLSI Technology", second edition, McGraw Hill (1988), pp. 493-494

George Fourson
Primary Examiner
Art Unit: 2823